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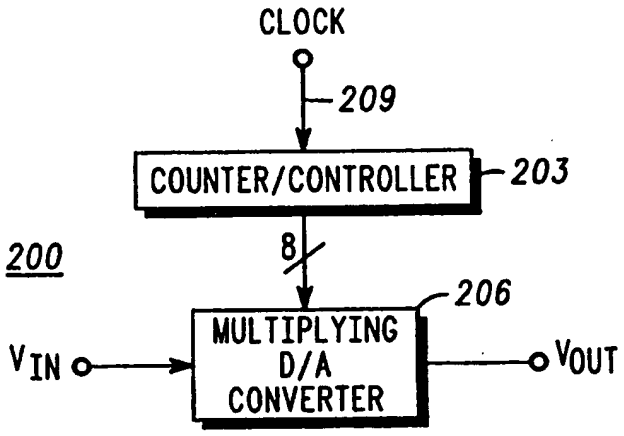
(57) Abstract

A digital-to-analog (D/A) convertor (206) multiplies an input signal by a sinewave approximation (300) to perform frequency translation. Optimized coefficient values are predetermined and are programmed based on a control word generated during a clock cycle. The programming over a time period representative of the frequency of the sinewave approximation (300) provides a signal that multiplies an input signal such that the effects of odd harmonics at an output are mitigated while the advantages of a traditional switching mixer are retained. In one embodiment the multiplying D/A convertor (206) includes a plurality of resistors (R1-R8) connected to an amplifier (400), with plural switching gates (G1-G8) switching select resistors (R1-R8) in and out of operation, a control word from counter/controller (203) controlling the gates (G1-G8).



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APPARATUS AND METHOD FOR FREQUENCY TRANSLATION IN A COMMUNICATION DEVICE

Field of the Invention

The present invention relates generally to communication devices and more specifically to frequency translation in communication devices.

Background of the Invention

In a Direct Conversion Receiver it is often necessary to upconvert the baseband signal to an IF frequency for demodulation. One of the most popular types of mixers that is used in the frequency range of 0-5 MHz is a switching mixer which uses CMOS transmission gates to alternately change the gain applied to the baseband signal between the values of +1 and -1. The gain is switched at a frequency of a local oscillator, F_{lo}.

Switching mixers have advantages such as simplicity, low offset voltage, large dynamic range, and easy to generate quadrature switching signals using D flip-flops. However, switching mixers have one major disadvantage in that the baseband signal will be replicated at each odd harmonic of the clock signal, due to the fact that the multiplying signal is a square wave. Since the harmonic rolloff rate of a square wave is 1/n, where n is the harmonic of F_{lo}, an undesired signal centered at $3F_{lo}$ will be present with a level that is approximately only 9.5 dB down from the desired signal centered at F_{lo}. As the bandwidth of the baseband signal approaches F_{lo}, a bandpass filter with very steep skirt selectivity is required in order to remove the undesired harmonic signals at $3F_{lo}$ and higher.

Since the baseband signal is multiplied by the Fourier Transform of the multiplying waveform, one obvious solution to reduce the odd harmonics which appear at the output of the mixer is to use a sinewave as the multiplying signal. There are several circuit approaches which exploit the nonlinearity of transistors to accomplish this technique, however, they do not have the advantages of the switching mixer which were mentioned above. Thus a need exists for a mixer having the advantages of the switching mixer described above without the having the disadvantage of the odd harmonics at its output.

Brief Description of the Drawings

FIG. 1 generally depicts in block diagram form a prior art switching mixer.

FIG. 2 generally depicts in block diagram form a switching mixer in accordance with the invention.

FIG. 3 generally depicts a square wave and a sinewave approximation in accordance with the invention.

FIG. 4 generally depicts an embodiment of a multiplying D/A convertor in accordance with the invention.

Detailed Description of a Preferred Embodiment

The proposed invention uses a multiplying digital-to-analog (D/A) convertor and a counter to generate a stair case type multiplying signal which approximates a sinewave with frequency equal to F_{lo}. In effect, the baseband signal is multiplied by several values other than just +1 and -1 as in the simple switching mixer. The D/A convertor is clocked at a frequency that is equal to NF_{lo} and the D/A convertor has N/2 steps (N/4 positive steps and N/4

negative steps). FIG. 3 shows a square wave 303 and a sinewave approximation 300 generated by the proposed invention with N=16.

If the step sizes of the multiplying D/A convertor are chosen properly, sinewave approximation 300 is good enough that several of the undesired harmonic signals may be set to zero (namely those that are closest to the desired signal). In most cases the mixer in accordance with the invention will eliminate the need for a high selectivity bandpass filter and will require only a simple lowpass filter to provide adequate attenuation to the harmonic signals which are not zero.

It can be shown that if the step sizes are chosen properly, the only harmonics of F_{lo} which appear at the output of the invention must satisfy the following equation.

$$n = iN \pm 1 \quad \text{where} \quad i = 0, 1, 2, 3.....$$

For the example that is shown (N=16), the first non zero undesired harmonic would be centered at $15F_{lo}$ compared to $3F_{lo}$ for the conventional switching mixer. There will be no undesired signals centered at $3F_{lo}$, $5F_{lo}$, $7F_{lo}$, $9F_{lo}$, $11F_{lo}$ and $13F_{lo}$ at the output of the mixer in accordance with the invention. This performance would not be achievable using any finite amount of selectivity following a switching mixer. The mixer in accordance with the invention gives infinite rejection to all harmonics between 2 and 14 (2 and N-2 for the general case) and will usually require only a simple lowpass filter to remove the 15th and higher harmonics. The mixer in accordance with the invention has all of the benefits of switching mixers mentioned above, as well as the added benefit of having reduced harmonic content.

A block diagram of a prior art switching mixer 100 is shown in FIG. 1. As stated above, the switching mixer 100 alternately changes the gain applied to the baseband signal Vin between the

values of +1 and -1 by amplifiers 103 and 106 respectively. Gates 109 and 112 are utilized to switch between amplifiers 103 and 106 at a rate F_{lo}. As stated above, this prior art switching mixer exhibits poor odd harmonic rejection at its output Vout.

FIG. 2 shows a block diagram of a switching mixer 200 in accordance with the invention. The gain applied to the baseband signal Vin is controlled by counter/controller 203 and a multiplying D/A convertor 206. The gain of multiplying D/A convertor 206 as a function of time is shown in FIG. 3 by the dotted sinewave approximation 300. Counter/controller 203 includes an up/down counter which automatically changes count direction when it has reached either its maximum or minimum value. For the example shown (N=16), the clock signal 209 has a frequency 16 times the desired frequency of sinewave approximation 300. Sinewave approximation 300 is approximated by 16 steps and due to its symmetry, 4 positive steps and 4 negative steps are required. The absolute value of the positive steps and the negative steps are equal. The symmetry of sinewave approximation 300 restricts the frequency of clock signal 209 to only integer multiples of 4 times the frequency of sinewave 300.

Since we have assumed that the frequency of clock signal 209 must be related to the frequency of sinewave approximation 300 by an integer multiple of 4 and that the same step sizes must be used in each quadrant of the square wave, the symmetry of the sinewave approximation 300 may be exploited in order to simplify the calculation of the Fourier Transform. Furthermore, sinewave approximation 300 has odd symmetry, we need only keep the sine terms in the calculation of the Fourier Transform. If we denote the sinewave frequency as ω_0, then the Fourier Transform of the multiplying waveform will be given by:

$$f(t) = \sum_{n=0}^{n=\infty} A_n \sin(n\omega_0 t)$$

where

$$A_n = \frac{2}{\pi}\int_0^{\pi} f(t)\sin(n\theta)\,d\theta$$

In the example that is shown in FIG. 3, there are four steps that are used to approximate the curvature of the sinewave. The step values are S_0, S_1, S_2 and S_3. In order to simplify the Fourier Transform calculation it is convenient to define a new set of variables. These variables are:

$$K_0 = S_0$$
$$K_1 = (S_1 - S_0)$$
$$K_2 = (S_2 - S_1)$$
$$K_3 = (S_3 - S_2)$$

The A_n coefficients may now be found in terms of the K_n coefficients as:

$$A_n = \frac{4}{n\pi}\sin\left(\frac{n\pi}{2}\right)\left[K_0\sin\left(\frac{4n\pi}{8}\right) + K_1\sin\left(\frac{3n\pi}{8}\right) + K_2\sin\left(\frac{2n\pi}{8}\right) + K_3\sin\left(\frac{n\pi}{8}\right)\right]$$

For the general case when N is not equal to 16 the A_n coefficients are:

$$A_n = \frac{4}{n\pi}\sin\left(\frac{n\pi}{2}\right)\left[\sum_{i=0}^{i=\frac{N}{4}-1} K_{\left(\frac{N}{4}-1-i\right)}\sin\left(\frac{2n\pi i}{N}\right)\right]$$

Three important observations may be made from an examination of the above equation.

$$A_n = 0 \quad \text{for even } n$$

$$A_{N+n} = A_n \text{ (except for the factor of } \frac{1}{n})$$

$$A_{N-n} = -A_n \text{ (except for the factor of } \frac{1}{n})$$

Due to the repetitive nature of the A_n coefficients and the fact that $A_{N-n} = -A_n$ (except for the factor of 1/n), we will consider only the first N/2 coefficients. Furthermore, since the even numbered coefficients are equal to zero, it is only necessary to consider the first N/4 odd coefficients. For the example given (N=16), the first N/4 odd coefficients are A_1, A_3, A_5 and A_7. The A_1 term gives us our desired mixing product, while the other terms give undesired harmonic signals which we will attempt to remove. Since there are 4 unknowns (the 4 step sizes), 4 of the A_n coefficients may be chosen arbitrarily. The first N/4 odd A_n coefficients are chosen as follows:

$$A_1 = 1.0$$
$$A_3 = 0.0$$
$$A_5 = 0.0$$
$$A_7 = 0.0$$

Due to the repetitive nature of the A_n coefficients the next N/4 odd A_n coefficients are given by:

$$A_9 = 0.0$$
$$A_{11} = 0.0$$
$$A_{13} = 0.0$$
$$A_{15} = \frac{-A_1}{n} = \frac{-1}{15}$$

Since there are N/4 unknowns (the K_n coefficients) and N/4 knowns (the A_n coefficients) a set of N/4 equations may be written

which relate the K_n coefficients to the A_n coefficients. These equations may be solved using any number of techniques. For the example given (N=16) the results are:

$$K_0 = 0.1963495408 \qquad S_0 = 0.1963495408$$
$$K_1 = 0.3628066440 \qquad S_1 = 0.5591561849$$
$$K_2 = 0.2776801836 \qquad S_2 = 0.8368363685$$
$$K_3 = 0.1502794325 \qquad S_3 = 0.9871158010$$

With this mixer design, the only non zero harmonics of the multiplying waveform which will appear at the mixer output, will be values of n which satisfy the following equation.

$$n = iN \pm 1 \quad \text{where} \quad i = 0, 1, 2, 3.....$$

The non zero A_n coefficients are related to A_1 in the same manner as the simple square wave.

$$|A_n| = \frac{|A_1|}{n}$$

In order to simplify the circuit design it is desirable to scale the step sizes so that the value of the maximum step size is equal to 1.0. The only effect that this simplification will have is a slight change in the gain of the mixer. For the example given (N=16) the new coefficients are:

$$S'_0 = 0.19891237$$
$$S'_1 = 0.56645450$$
$$S'_2 = 0.84775907$$
$$S'_3 = 1.00000000$$

These coefficients are shown in FIG. 3. The table shown below gives the first 31 harmonic levels for the conventional

switching mixer and the new mixer (N=16). The harmonic levels are given in dB relative to the desired harmonic (n=1). The even order harmonics are not shown since they are zero ($-\infty$ dB) for both mixers.

n	Conventional Mixer	New Mixer
1	0.00	0.00
3	− 9.54	$-\infty$
5	− 13.98	$-\infty$
7	− 16.90	$-\infty$
9	− 19.08	$-\infty$
11	− 20.83	$-\infty$
13	− 22.28	$-\infty$
15	− 23.52	− 23.52
17	− 24.61	− 24.61
19	− 25.56	$-\infty$
21	− 26.44	$-\infty$
23	− 27.23	$-\infty$
25	− 27.96	$-\infty$
27	− 28.63	$-\infty$
29	− 29.25	$-\infty$
31	− 29.83	− 29.83

TABLE 1

FIG. 4 generally depicts the predetermined circuitry of the preferred embodiment of multiplying D/A convertor 206 in accordance with the invention. As shown in FIG. 4 a plurality of resistors designated by resistors R1-R8 are connected to an amplifier 400. Switching gates G1-G8 are utilized to switch resistors R1-R8 into and out of the predetermined circuitry via a control word output by counter/controller 203. In the preferred

embodiment, the control word is a 3-bit control word. Also in the preferred embodiment, resistors R1 and R8 = 15.22 KΩ, R2 and R7 = 28.13 KΩ, R3 and R6 = 36.76 KΩ and R4 and R5 = 19.89 KΩ which, when programmed, yield coefficients S_0'-S_3' calculated above.

Operation of predetermined circuitry 206 which comprises multiplying D/A convertor 206 is as follows. Clock signal 209 having a predetermined clock cycle rate ($16F_{lo}$ in the preferred embodiment) is input into counter/controller 203. For every clock cycle, counter/controller 203 outputs a predetermined control word based on the coefficients S_0'-S_3' as calculated above. For a given control word, gates G1-G8 switch into and out of certain resistors R1-R8 based on the control word. This yields a certain multiplication ratio for circuitry 206 which changes every clock cycle as the control word changes. Consequently, the result of circuitry 206 changing every clock cycle is that an input signal Vin is multiplied by step sizes (based on the coefficients S_0'-S_3' as calculated above) which, as a function of time, approximate sinewave approximation 300. In this manner, the advantages of a switching mixer are obtained without the exhibition of odd harmonics at the output of the mixer.

What we claim is:

Claims

1. An apparatus for frequency translation comprising:

a clock signal having a predetermined clock cycle rate;

a controller for outputting a predetermined control signal every clock cycle; and

a multiplying digital-to-analog convertor having a multiplication ratio based on the control signal, the multiplying digital-to-analog convertor multiplying an input signal by step sizes which, as a function of time, approximate a sinewave.

2. The apparatus of claim 1 wherein the control signal further comprises a control word.

3. The apparatus of claim 2 wherein the multiplication ratio based on the control word further comprises switching a plurality of resistors into and out of predetermined circuitry via a plurality of switches, the plurality of switches controlled by the control word.

4. The apparatus of claim 3 wherein the step sizes are non-linear and are optimally determined based on switching a plurality of resistors having optimized values into and out of predetermined circuitry via the plurality of switches controlled by the control word.

5. The apparatus of claim 1 wherein the step sizes which approximate a sinewave as a function of time further comprise step sizes which approximate a sinewave over 16 clock cycles.

6. A method of frequency translation comprising:

providing a clock signal having a predetermined clock cycle rate;

outputting a predetermined control signal every clock cycle; and

multiplying an input signal by a multiplication ratio based on the control signal, the multiplication ratio related to step sizes which, as a function of time, approximate a sinewave.

7. The method of claim 6 wherein the control signal further comprises a control word.

8. The method of claim 7 wherein the step of multiplying an input signal by the multiplication ratio based on the control word further comprises the step of switching a plurality of resistors into and out of predetermined circuitry via a plurality of switches, the plurality of switches controlled by the control word.

9. The method of claim 8 wherein the step sizes are non-linear and are optimally determined based on switching a plurality of resistors having optimized values into and out of predetermined circuitry via the plurality of switches controlled by the control word.

10. The method of claim 6 wherein the step sizes are linear step sizes.

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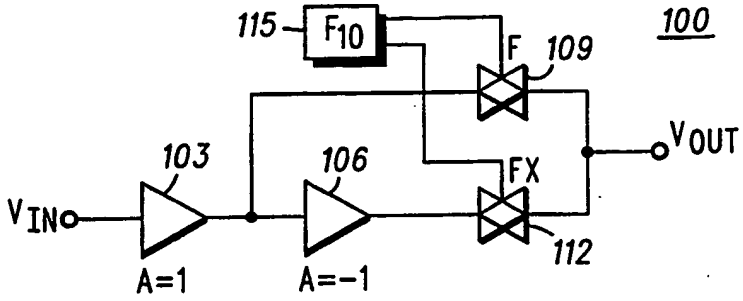


FIG.1
— PRIOR ART —

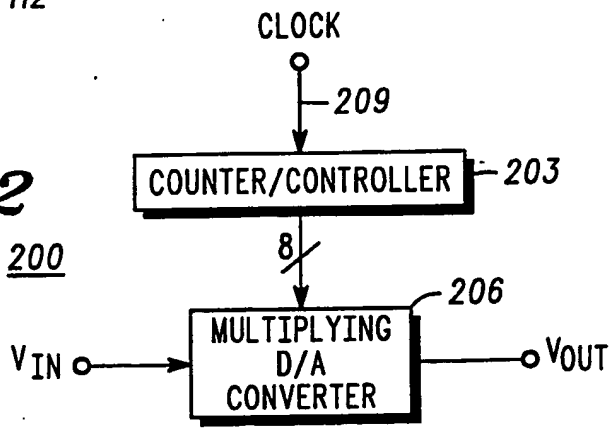


FIG.2

FIG.3

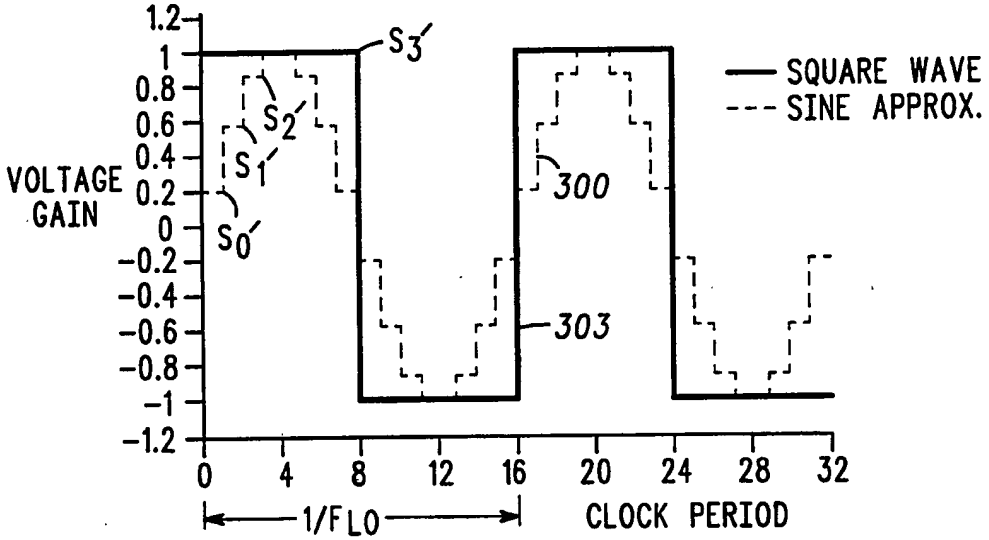
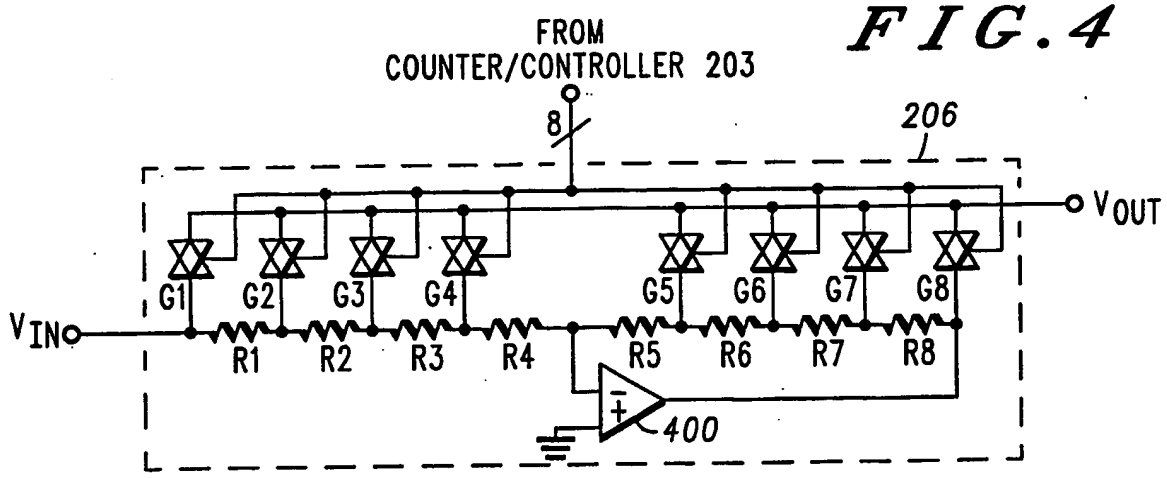


FIG.4



INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H03M 1/66
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According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 341/144, 147, 61

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
search terms: multiplying dac, sine approximation, frequency

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 4,727,752 (PETERS) 01 March 1988, col. 5-7.	1-4, 6-10
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